Taking the matters raised by the examiner in turn, regarding numbered paragraph 1 on page 2 of the office action, Figure 1a has been designated as prior art. Figure 1b is not prior art, however, and has not been designated as such. It is a proposed energy level diagram that has been prepared by the applicants.

Regarding numbered paragraph 2, reference 236 has been added to Figure 2b.

Regarding numbered paragraph 3, reference numeral 214 has been deleted from Figure 1b, reference 301 has been deleted from Figure 3, a description of reference sign 705 has been added to the specification, a description of reference sign 174 has been added to the specification and reference sign 2009 has been deleted from figure 15.

Regarding numbered paragraph 4, the specification has been clarified to make it clear that reference 402 refers to the insulating layer in general, and reference 413 refers to those portions of it between the particle analogs 411. It is believed that everything is now in order.

Regarding the specification, headings have been added to the specification where appropriate. Also, the description of Figures 1a and 1b has been added, and the title has been changed to that proposed by the examiner. Thus, paragraphs 7 through 10 of the office action have been satisfied.

Regarding the objection to claims 60 and 61 in numbered paragraph 11, the error in the claims has been corrected.

In numbered paragraphs 12 through 63 beginning on page 4 of the office action, the examiner has rejected claims 1 – 61 under 35 U.S.C. §103 as being obvious over Tuck U.S. Patent Number 6,097,139. Reconsideration is requested.

In Tuck et al (USPN 6097139), there is disclosed an emitter having a MIMIV structure (metal-insulator-metal-insulator-vacuum). This requires an insulator layer at two different locations on the conductive particle, to achieve emission. Current has to flow through the insulator at the first location and then through the particle itself and then through the insulator at the second location.

The emission process is described in Tuck et al from col. 2, line 49. This states a three stage process: 1) The formation of a channel between the particle and the substrate due to the antenna effect, 2) the change in potential of the particle, and then 3) the formation of the MIV channel at the top of the particle.

Thus, the teaching of Tuck et al is wholly and consistently that, in order to obtain emission, current paths must be provided through the insulator in two locations, one at the substrate and one at the vacuum.

There is no reason whatsoever for the reader to suppose from Tuck et al that one of the current paths through the insulator might be dispensed with. This would be at variance with the teachings of Tuck et al. There would be no three-stage process as taught.

In the present application, it is disclosed that, surprisingly, emission may be obtained with a MIV structure in two possible formats, which we can refer to conveniently as MIV I and MIV II:

In MIV I, the channel is at the base of the particle. Here the channel is formed by the antenna effect (similar to stage one in the MIMIV emitter), but then goes on to emit electrons by virtue of a different mechanism that is not obvious from the MIMIV physics. That is that the particle begins to charge and no further current flows into the particle. However, electrons are then emitted into the vacuum directly from the channel in the vicinity of the charged particle. This process is described in the present application.

In MIV II, the channel is formed on the top of the particle because the particle has a geometrical field enhancement factor governed by its morphology. The particle remains at the same potential as the back contact throughout, and does not undergo a sudden change in potential, as is the case with the MIMIV structure. This process is described in the present application.

Thus, from a consideration of the MIMIV physics of Tuck et al, it is not at all obvious that an emitter can be formed as claimed in the present application.

It may be observed that neither the EPO nor GB Examiner has raised a rejection. The GB application has been granted (GB 2 332 089) and the EP application is proceeding to grant (EP 1 036 402).

Given the above, it is submitted that this application is now in condition for allowance, and the examiner's further and favorable reconsideration in that regard is urged.

As this response is being filed during the fourth month following the examiner's office action (January 5, 2003 being a Sunday), an appropriate petition for extension of time is submitted herewith.

Finally, certain prior art has been cited in the corresponding British applications, but not in the present application or the corresponding PCT application. Therefore, to fulfill the duty of disclosure, an Information Disclosure Statement is submitted herewith along with the fee of $180 pursuant to 37 C.F.R. §1.17(p).

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Respectfully submitted,

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Version With Markings To Show Changes Made

Page 14, lines 3 –7:

Brief Description of the Drawings

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to [Figures 2 to 19 of] the accompanying diagrammatic drawings, in which:

Figure 1a illustrates a known emission mechanism in which a conducting flake sits on an insulating layer;

Figure 1b is a proposed energy level diagram for an electro-formed conducting channel in the insulating layer of Figure 1a;

Page 19, lines 3 – 15:

Figure 4 shows an alternative method of making an emitter in which a conducting substrate 401 has a layer of insulator 402 and conductor 403 deposited upon it. Using, for example, a patterned resist layer 404, the conducting material 402 is selectively etched 412 to leave fabricated particle analogues 411. In some cases it may be advantageous to also remove the portions 413 of insulating layer [413] from between the particle analogues. The natural tendency for etching to form undercuts 415 below the resist pattern 404 facilitates the exit of electrons 416 from the electro-formed channel at the base of the structure. Said structures may be also constructed using the well established techniques of semiconductor fabrication. For example the insulating layer 402 may be formed by oxidising an otherwise conducting wafer and then metallised. A similar approach may be used to form the structures illustrated in Figure 2b.

Page 21, lines 18 – 23:

Figure 7 shows a useful process in which Step 1 a substrate 701 with insulator 702 and particles 703 has an area masked by a resist coating 704. In Step 2 a selective etch is used to remove the particles. In Step 3 the resist is removed to leave the masked areas 705 with field emitting properties.

Page 29, lines 4 – 25:

In Figure 13 a glass plate 170 has an optically transparent electrically conducting coating 171 (for example, tin oxide) onto which is formed a layer of MIV emitter 172 as described herein. This emitter is formulated to be substantially optically translucent and, being comprised of randomly spaced particles, does not suffer from the Moire patterning that the interference between a regular tip array and the pixel array of an LCD would produce. Such a layer may be formed with, although not limited to, a heat cured polysiloxane based spin-on glass as the insulating component. The coated cathode plate described above is supported above an anode plate by spacers 179 and the structure sealed and evacuated in the same manner as the lamp shown in Figure 10a. The anode plate 177 which may be of glass, ceramic, metal or other suitable material has disposed upon it a layer of a electroluminescent phosphor 175 with an optional reflective layer 176, such as [aluminium]aluminum, between the phosphor and the anode plate. A voltage 180 in the kilovolt range is applied between the conducting layer 171 and the anode plate 177 (or in the case of insulating materials a conducting coating thereon). Field emitted electrons 173 caused by said applied voltage are accelerated to the phosphor 175. The resulting light output 174 passes through the translucent emitter 172 and transparent conducting layer 171. An optional Lambertian or

non-Lambertian diffuser 178 may be disposed in the optical path. Similar approaches may be used to increase the luminance of addressable displays.

Claims:

60. (Amended) A method according to claim 24, wherein said conducting layer [compromises]comprises a metal conducting element or compound, semiconductor or composite.

61. (Amended) A method according to claim 25, wherein said conducting layer [compromises]comprises a metal conducting element or compound, semiconductor or composite.